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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
SHUTE, DOUGLAS M

ART UNIT	PAPER NUMBER
2121	5

DATE MAILED: 06/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/666,456	MIYAMORI, TAKASHI	
	Examiner	Art Unit	
	Douglas M. Shute	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 January 2003* .

2a)☐ This action is FINAL. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☒ Claim(s) *19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-19 are presented for examination.

Claim Objections

2. Claim 19 is objected to because of the following informalities: The limitation ", and invalidates the execution result of the arithmetic operation in said processor core" found at the end of the claim is redundant. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 8, 11, and 18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the

art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

5. Re claim 11, it is rejected since the limitations therein are unclear and merely repeat the respective portion of the specification (page 6, lines 13-19).

6. Re claims 8 and 18, they are rejected since the corresponding portion of the specification (page 5, lines 29-33) is unclear. The specification recites "suspending execution of an instruction inputted from the extended arithmetic unit". It is unclear here whether it is the stop signal or the instruction which is being inputted from the extended arithmetic unit.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 3 and 4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Claim 3 recites the limitation "the instruction decoded is said extended arithmetic unit control instruction". There is insufficient antecedent basis for this limitation in the claim.

10. Claim 4 recites the limitation "said extended arithmetic unit control instruction". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

12. Claim 1 is rejected under 35 U.S.C. 102(a) as being anticipated by Nishigami (5,890,010) (hereinafter Nishigami).

13. As per claim 1, Nishigami shows a processor, comprising: a processor core (e.g., figure 1, element 1); a data memory accessed by said processor core (e.g., figure 1, element 3); and an extended arithmetic unit, connected to an exterior of said processor core (e.g., figure 1, element 2), for processing a particular instruction, said extended arithmetic unit executing an arithmetic operation by using arithmetic operation data retained in a register file in said processor core (e.g., figure 1, element 5 and col. 6 , lines 48-57), and outputting a result of an arithmetic operation directly to said processor core (e.g., figure 1, element 14), said processor core saving the result of the arithmetic operation executed by said extended arithmetic unit and inputted therefrom in said register file in said processor core (e.g., figure 1, element 5 and col. 6, lines 48-57).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 4, 9, 11, 14, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishigami.

16. As per claim 4, as best understood, it is rejected for reasons given above for claim 1. In addition, Nishigami shows the use of register numbers to designate a particular register for data transfer to the coprocessor (e.g., col. 6., lines 48-57). However, Nishigami does not specifically show the said arithmetic operation data outputted to said extended arithmetic unit is

a value read out from said register file in said processor core in accordance with a register number specified by a part of said extended arithmetic unit control instruction. It would have been obvious to one of ordinary skill in the art at the time the

invention was made that the source of the register number utilized for data transfer to the coprocessor could have been a portion of the extended arithmetic unit control instruction as address information is a well known and frequently occurring component of an instruction.

17. As per claim 14, it is rejected for reasons similar to those above for claim 4.

18. As per claim 9, it is rejected for reasons given above for claim 1 and further as it would have been obvious to one of ordinary skill in the art at the time the invention was made that said extended arithmetic unit could output to said processor core an arithmetic operation result invalidating signal that invalidates an execution result of an arithmetic operation executed in said processor core. A well known example of this would be to utilize an error signal produced by an improper result of the extended arithmetic unit to indicate that a related calculation in the processor core was also incorrect.

19. As per claim 19, it is rejected for reasons similar to those of claim 9 above.

20. As per claim 11, as best understood, it would have been obvious to one of ordinary skill in the art at the time the invention was made that said extended arithmetic unit could include:
a plurality of arithmetic circuits;
a first pipeline register for storing a processing result by an arithmetic circuit in a preceding stage at a rising of a following clock; and a second pipeline register for storing a processing
result by an arithmetic circuit in a succeeding stage at the rising of the following clock since this would represent a common pipeline processing structure.

21. Claims 2, 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishigami in view of Laborie (6,003,124) (hereinafter Laborie).

22. As per claim 2, Nishigami shows the invention substantially as claimed having a processor, comprising: a processor core (e.g., figure 1, element 1); a data memory accessed by said processor core (e.g., figure 1, element 3); and an extended arithmetic unit, connected to an exterior of said processor core,

for processing a particular instruction (e.g., figure 1, element 2), in case that an instruction is an extended arithmetic unit control instruction that should be executed by said extended arithmetic unit connected to the exterior of said processor core, also outputting
at least an instruction code of said extended arithmetic unit control instruction to said extended arithmetic unit (e.g., col.2, lines 3-10); a register file for retaining arithmetic operation data of an arithmetic operation that should be executed by the instruction (e.g., figure 1, element 5 and col. 6, lines 48-57), in case that said arithmetic operation data is data of said extended arithmetic unit control instruction, said register file also outputting said arithmetic operation data to said extended arithmetic unit (e.g., figure 1, element 5 and col.6, lines 48-57); a first operational section for executing the instruction decoded (e.g., figure 1, element 9); and an extended arithmetic unit (e.g., figure 1, element 2), at least including, a second operational section for executing an arithmetic operation specified by said extended arithmetic unit control instruction by using said arithmetic operation data retained in said register (e.g., figure 1, element 8), and outputting an execution result of the arithmetic operation to said processor core (e.g., figure 1, element 14). Nishigami does not

specifically show a processor core at least including: an instruction memory for storing an instruction to be executed and an instruction decode unit for reading out an instruction from said instruction memory to decode the instruction. Laborie shows these processor core elements (e.g., figure 1, elements 6 and 7). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the instruction handling elements of Laborie in Nishigami as these are well known processing elements in a computer system which utilizes instructions.

23. As per claim 12, it is rejected for reasons similar to those above for claim 2.

24. As per claim 10, it is rejected for reasons similar to those for claim 1 above. However, Nishigmi does not specifically show that the data

memory:

receives from said extended arithmetic unit at least one of an address for memory access, data, a write control signal for controlling data writing, and a read control signal for controlling data reading;

reads out the data from a region specified by said address

and outputs the data to said extended arithmetic unit in case that data reading is carried out because said read control signal is asserted: and

writes the data inputted from said extended arithmetic unit into a region specified by said address in case that data writing is carried out because said write control signal is asserted. However, Laborie shows (e.g., col. 6, lines 15-21) external memory accessing by the coprocessor (extended arithmetic unit). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the memory accessing of Laborie in the system of Nishigami in order to provide access to additional data for the extended arithmetic unit as a particular circumstance warranted. It would have been further obvious to one of ordinary skill in the art at the time the invention was made to utilize the remaining specifics of memory accessing recited in the claim above (e.g., address, read control, write control) as these are well known mechanisms for accessing any memory system.

25. Claims 3 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishigami in view of Nguyen et al. (5,961,628)(hereinafter Nguyen).

26. Re claim 3, as best understood, it is rejected for reasons similar to those of claim 1 above. Also, Nishigami does not specifically show in case that the instruction decoded is said extended arithmetic unit control instruction, said processor core outputs to said extended arithmetic unit at least an instruction code that specifies an action involved in an arithmetic operation in said extended arithmetic unit and an instruction valid signal that indicates said instruction code is valid. However, Nguyen shows the utilization of an instruction valid signal along with normal instruction processing (e.g., col. 13, lines 13-18). It would have been obvious to one of ordinary skill in the art at the time the invention was made that the instruction valid signal of Nguyen could be utilized in Nishigami in order to enhance the confidence and reliability in instruction processing.

27. As per claim 13, it is rejected for reasons similar to those of claim 3 above.

28. Claims 5, 6, 7, 8, 15, 16, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishigami in view of Williams (5,774,704)(hereinafter Williams).

29. As per claim 5, it is rejected for reasons given above for claim 1. Also, Nishigami does not specifically show said processor core includes a pipeline control unit for controlling pipeline processing in an interior of said processor core and in said extended arithmetic unit. However, Williams shows the use of pipeline control in as system having a CPU (e.g., figure 2, element 204) and a floating point unit (extended arithmetic unit) (e.g., figure 2, element 203). It would have been obvious to one of ordinary skill in the art at the time the invention was made that the pipeline system of Williams could be used in Nishigami to provide a more efficient processing of instructions therein.

30. As per claim 15, it is rejected for reasons similar to those of claim 5 above.

31. As per claim 6, it is rejected for reasons similar to those of claim 5 above. Further, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the pipeline control unit could output to said extended arithmetic unit a first pipeline stop signal for suspending execution of an instruction in said extended arithmetic unit as this is a typical pipeline processing operation.

32. As per claim 16, it is rejected for reasons similar to those of claim 6 above.

33. As per claim 7, it is rejected for reasons similar to those of claim 5 above. Further, it would have been obvious to one of ordinary skill in the art at the time the invention was made that said pipeline control unit could output to said extended arithmetic unit a pipeline flush signal for abandoning execution of an instruction outputted to said extended arithmetic unit as this is a typical pipeline processing operation.

34. As per claim 17, it is rejected for reasons similar to those of claim 7 above.

35. As per claim 8, as best understood, it is rejected for reasons similar to those of claim 5 above. Further, it would have been obvious to one of ordinary skill in that art at the time the invention was made that a pipeline control unit could suspend execution of an instruction in the processor core in accordance with a second pipeline stop signal from said extended arithmetic unit and executed by said processor core since such suspension is a typical pipeline processing operation and the source of a stop

signal could be either the processor core or the extended arithmetic unit as a particular circumstance warranted.

36. As per claim 18, as best understood, it is rejected for reasons similar to those of claim 8 above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas M. Shute whose telephone number is (703) 305-5615. The examiner can normally be reached on M-F 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Follansbee can be reached on (703) 305-8498. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-9600.

June 6, 2003

RAMESH PATEL 6/8/03
PRIMARY EXAMINER
For John Follansbee